

Fig. 1





### MV Interface Description

This interface uses additional pins to provide Tag/mode selection info for future implementations of high latency RDC designs with latency could be more than one sector long

### MCMD timing chart for Write/Read operations

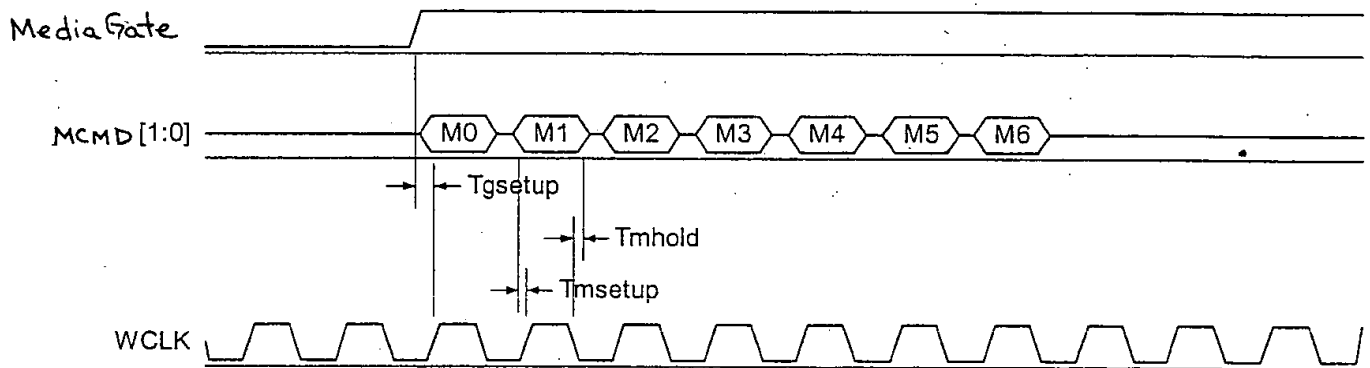


Fig. 3



## High latency write

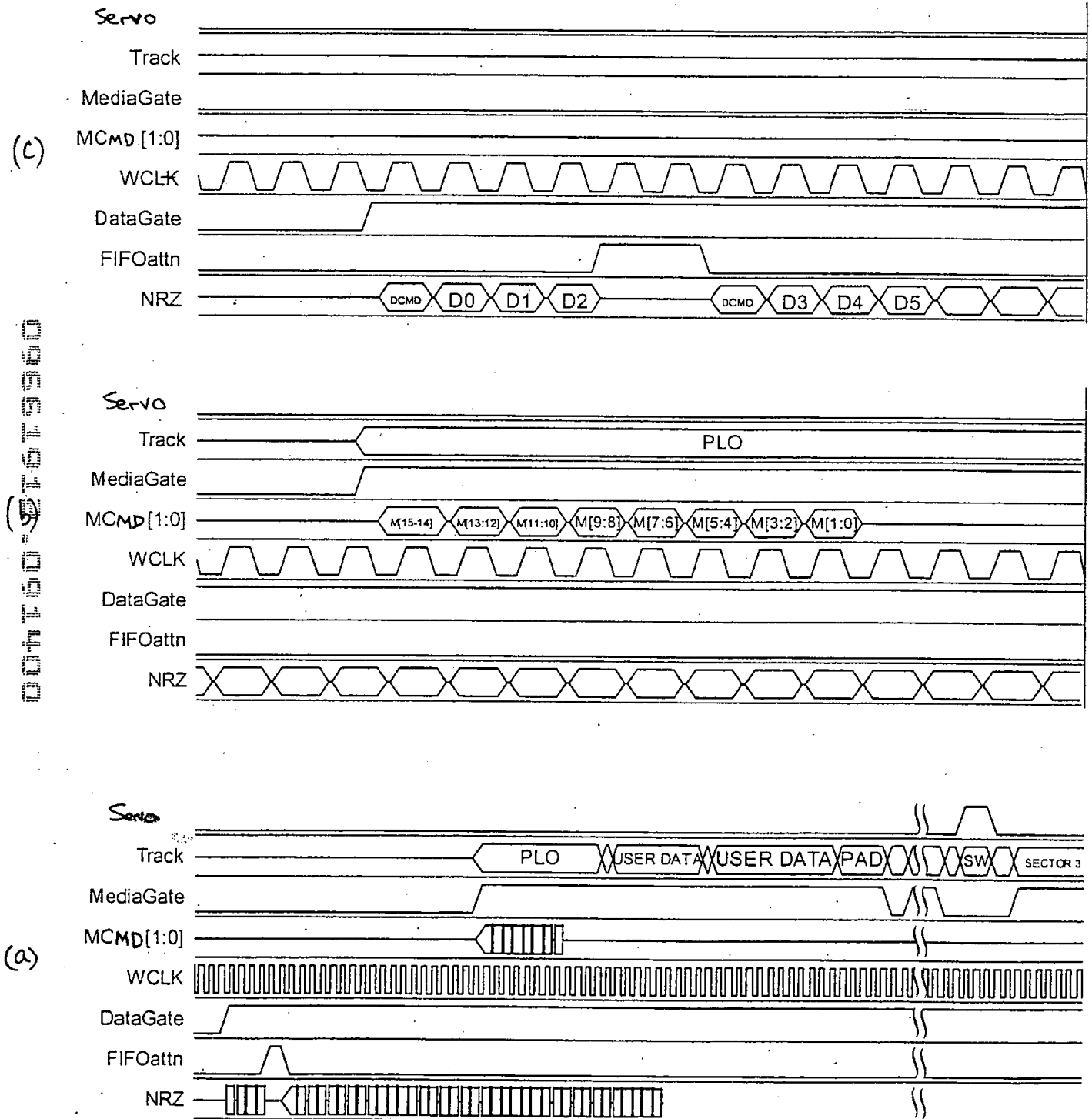


Fig. 4

[illegible]

(c)

The diagram shows the following signal behavior:

- Servo**: A constant high signal.
- Track**: A signal that transitions from low to high at the start of the PLO period and remains high until the Sync signal.
- MediaGate**: A signal that transitions from low to high at the start of the PLO period and remains high until the Sync signal.
- MCMD[1:0]**: A signal that transitions from low to high at the start of the PLO period and remains high until the Sync signal.
- WCLK**: A periodic clock signal.
- DataGate**: A signal that transitions from low to high at the start of the PLO period and remains high until the Sync signal.
- FIFOattn**: A signal that transitions from low to high at the start of the PLO period and remains high until the Sync signal.
- NRZ**: A signal that transitions from low to high at the start of the PLO period and remains high until the Sync signal.

(b)

The diagram shows the following signals and their states:

- Servo**: High throughout the entire duration.
- Track**: Low initially, then transitions to high during the 'Data' period, and returns to low.
- MediaGate**: Low throughout the entire duration.
- MCMD[1:0]**: High throughout the entire duration.
- WCLK**: A continuous periodic square wave.
- DataGate**: Low initially, then transitions to high during the 'Data' period, and returns to low.
- FIFOattn**: Low throughout the entire duration.
- NRZ**: A serial data stream. It starts with a sync pulse, followed by data bytes D1 through D8, then another sync pulse, followed by data bytes D9 through D11, and ends with two more sync pulses.

(a)

Timing diagram for a servo system. The signals shown are:

- Servo
- Track
- MediaGate
- MCMD[1:0]
- WCLK
- DataGate
- FIFOattn
- NRZ

The diagram illustrates the sequence of operations, including PLO, Data, pad, SW, and Data3 blocks, and the MediaGate pulse. The NRZ signal shows two bursts of data.

Fig. 5